In The Claims

Please amend the claims as follows:

Listing of Claims:

Claim 1 (currently amended). A calculation circuit for the division of a fixed-point input signal, which comprises a sequence of digital data values having a width of *n* bits, by an adjustable division factor 2^a for generating a divided fixed-point output signal, the circuit comprising:

a signal input for receiving a data value sequence of the fixed-point input signal;

a first addition circuit for adding the digital data value input at the signal input to a data value stored in a register to form a digital first summation data value comprising a width of max (*n*, *a*+1) +1 bits;

a shift circuit for shifting the first summation data value by *a* data bits towards the right to output the max (*n*, *a*+1) -a+1 more significant data bits of the first summation data value;

a logic circuit having an AND gate configured to logically AND ~~for logically ANDing~~ the *a* less significant data bits of the first summation data value with a logic combination data value to generate a first logically combined data value (d_{v1}) and having an OR gate configured to logically OR~~, or logically ORing~~ the *a* less significant data bits of the first summation data value with an inverted logical combination data value to generate a second logically combined

data value (d_{v2}) wherein~~,~~ depending on a sign of the first summation data value the first logically combined data value (d_{v1}) or the second logically combined data value (d_{v2}) is output~~, and for outputting a logically combined data value~~ for storage in the register;

a second addition circuit configured to provide as an output ~~for adding~~ the data value output by the shift circuit added to a value one for eliminating the DC signal component to form a second summation data value, depending on a sign of the first summation data value; and

a signal output for outputting the sequence of the second addition circuit output ~~summation data value~~ as a divided fixed-point output signal.

Claim 2 (original). The calculation circuit of claim 1 further comprising a sign identification circuit for identifying a sign of the first summation data value.

Claim 3 (original). The calculation circuit of claim 1, wherein the logic combination data value is equal to the division factor reduced by the value one.

Claim 4 (original). The calculation circuit of claim 1, wherein the logic circuit comprises an inverter for inverting the logic combination date value.

Claims 5 and 6 (cancelled).

Claim 7 (currently amended). The calculation circuit of claim 2~~6~~, wherein the logic circuit comprises a multiplexer, the multiplexer comprising:

a first input, which is connected to the output of the AND gate,

a second input, which is connected to the output of the OR gate,

an output, which is connected to the register, and

a control input, which is driven by a sign identification circuit.

Claim 8 (currently amended). The calculation circuit of claim 2~~1~~, wherein the second addition circuit comprises:

an adder for adding the data value output by the shift circuit to the value one to form the second summation data value; and

a multiplexer, which, as a function of a control signal received from the~~a~~ sign identification circuit, switches through the data value or the second summation data value, generated by the ~~second~~ adder, to the signal output of the calculation circuit.

Claim 9 (original). The calculation circuit of claim 8, wherein when a positive sign of the first summation data value is identified by the sign identification circuit, the multiplexer of the second addition circuit switches through the data value output by the shift circuit to the signal output of the calculation circuit, and when a negative sign of the first summation data value is identified by the sign identification circuit, the multiplexer of the second addition circuit switches through the second summation data value output by the adder to the signal output of the calculation circuit.

Claim 10 (currently amended). The calculation circuit of claim 1, wherein when a positive sign of the first summation data value is identified by a sign identification circuit, ~~the~~a multiplexer of the logic circuit switches through the output of the AND gate to the register, and when a negative sign of the first summation data value is identified by the sign identification circuit, the multiplexer of the logic circuit switches through the output of an OR gate to the register.

Claim 11 (currently amended). The calculation circuit of claim 3~~1~~, wherein the division factor is a power value with a base 2 and an exponent *a*.

Claim 12 (original). The calculation circuit of claim 11, wherein the exponent *a* corresponds to the number of data bits shifted toward the right by the shift circuit.

Claims 13-18 (canceled).

Claim 19 (currently amended). A method for dividing a fixed-point input signal, which comprises a sequence of digital data values having a width of *n* bits, by an adjustable division factor 2^a for generating a divided fixed-point output signal, the method comprising the steps of:

receiving a data value sequence of the fixed-point input signal;

adding the digital data value of the fixed-point input signal to a ~~stored~~ data value stored in a register to form a digital first summation data value comprising a width of max (*n*, *a*+1) +1 bits;

shifting the first summation data value by *a* data bits towards the right to generate the max (*n*, *a*+ I) -*a*+1 more significant data bits of the first summation data value;

logically ANDing the *a* less significant data bits of the first summation data value with a logic combination data value using an AND gate to generate a first logically combined data value (d_{v1}), or logically ORing the *a* less significant data bits of the first summation data value with an inverted logical combination data value using and OR gate to generate a second logically combined data value (d_{v2}), wherein~~,~~ depending on a sign of the first summation data value, the first log first logically combined data value (d_{v1}) or the second logically combined data value (d_{v2}) is output for storage in the register ~~to generate a logically combined data value~~;

adding a value one to the shifted first summation data value for eliminating the DC signal component to form a second summation data value, depending on a sign of the first summation data value; and

outputting the sequence of the second summation data value as a divided fixed-point output signal.